

FAX TRANSMISSION**RECEIVED**
CENTRAL FAX CENTER**APR 26 2004****OFFICIAL****DATE:** April 26, 2004**PTO IDENTIFIER:** Application Number 09/588,351-Conf. #8116
Patent Number**Inventor:** Roy C. (deceased), Flaker et al.**MESSAGE TO:** US Patent and Trademark Office**FAX NUMBER:** (703) 872-9306**FROM:** CONNOLLY BOVE LODGE & HUTZ LLP

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PHONE: (202) 331-7111**Attorney Dkt. #:** 20136-00305-US**PAGES (Including Cover Sheet):** 6**CONTENTS:** Response to After Final Action (37 C.F.R. Section 1.116) (4 pages) and
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APR 26 2004

OFFICIALDocket No.: 20136-00305-US
(PATENT)**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of:
Roy C. (deceased), Flaker et al.

Application No.: 09/588,351

Confirmation No.: 8116

Filed: June 7, 2000

Art Unit: 2815

For: CIRCUIT AND METHODS TO IMPROVE
THE OPERATION OF SOI DEVICES

Examiner: J. A. Fenty

RESPONSE AFTER FINAL REJECTION UNDER 37 C.F.R. 1.116

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Final Rejection mailed February 24, 2004, favorable reconsideration is requested in light of the remarks which follow.

REMARKS

Claims 6-14 are pending in the application. Favorable reconsideration is requested.

Withdrawal of the rejection of claims 6-14 under 35 U.S.C. §102(e) as being anticipated by Okumura et al. (U.S. Patent No. 5,892,260) is requested. The present invention is directed to a method to enhance the performance of a circuit formed as a SOI device. As set forth in the specification, a disadvantage with SOI devices is that electrical charge accumulates in the body of the device until the electrical potential increases sufficiently to produce a shift in the threshold voltage of the device. The shift adversely effects the operation of the circuit and introduces errors into the information being processed by the device.

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The present invention avoids the consequences of the accumulated charge build-up by using a method which discharges the accumulated electrical charge just prior to the time the SOI device is being accessed. Once the accumulated charge has been dissipated, the speed penalty for successive accesses of an SOI fabricated device is eliminated.

The Okumura et al. patent discloses an apparatus and method which changes the bias voltage on a substrate, depending upon whether the device is in a stand-by or active mode. Referring to Figure 4 of the reference, a bias voltage generator 312 causes the voltage of a back gate region 305 of the P-channel transistor to be V_{DD} which increases the absolute value of the threshold voltage. When the active mode is entered, the bias voltage generating circuit 312 causes the voltage of the back gate region 305 to be a voltage V_1 which is lower than V_{DD} and higher than $V_{DD}-V_F$, thus decreasing the absolute value of the threshold voltage. (See col. 6, lines 17-27). The purpose of the bias voltage generating circuit increases the threshold voltages in a standby mode so that the sub threshold currents, and corresponding power dissipation, can be reduced. During the active mode the absolute values of the threshold voltages are decreased so as to increase the operation speed. (See col. 6, lines 38-43).

The effect is to control the threshold voltage so that operation speed is increased and power dissipation is increased when the bias voltage is active. On the other hand, in a standby mode, the substrate voltage is zero to raise the threshold voltage so that the threshold current is decreased to decrease the power dissipation (See col. 4, lines 7-14).

The rejected claims are clearly distinguishable from the foregoing. For instance, the references fails to disclose a pulse discharge circuit. Instead, it shows a bias circuit which can be controlled to be on and off, for biasing the circuit one way, or the other, to decrease power dissipation or decrease the threshold voltage during an operational sequence. Nothing appears to be disclosed in the reference which would discharge any accumulated potential on the body of at least one SOI device. Accordingly, the feature of Applicants' claims which requires that the accumulated potential be discharged prior to accessing at least one SOI device is not suggested in the reference. While the reference does disclose biasing the substrate of a device in a standby mode, for minimizing power dissipation, and for lowering the threshold voltage in an active

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mode such that it responds to a rapid switching signal, the two functions are not identical to discharging potential on a body before accessing a SOI device.

Withdrawal of the rejection of claims 6-14 under the judicially created doctrine of obviousness type double patenting as being unpatentable over claims 1-4 of Flaker in view of Okumura is requested. The allegation that it "would have been obvious for one skilled in the art to connect the pulse discharge circuit directly to the body region of Flaker, as disclosed by Okumura for the purpose, for example, of enhancing the speed of the device while decreasing the power dissipation" is not supported by the proposed combination of references. Specifically, Okumura discloses biasing a circuit element so that it decreases power dissipation in a standby mode. This is the result of changing threshold voltages of the device, such that an increased threshold voltage produces less power dissipation.

The present invention, as set forth in the rejected claims, requires that prior to accessing a SOI device, the substrate be discharge. Accordingly, Okumura does not suggest discharging the substrate for removing any access charge, but biases the substrate so that in a standby mode there is little power dissipation. The combination of steps in the rejected claims require that prior to accessing a SOI device, the accumulated charge on the substrate be discharged. In this manner, the prior art SOI devices do not suffer from the drawbacks of an accumulated charge which interferes with the switching of the device on and off.

In a judicially created double patenting rejection, it is the claims of the earlier patent which are used in combination with other prior art to reject the application. In looking at the claims of the prior patent, there is no indication that the step of applying the pulse prior to accessing a device, as set forth in each of the currently rejected claims would be obvious from claims 1-4 of Flaker et al. Accordingly, this reference when combined with Okumura can not yield or suggest the claims.

In view of the foregoing, favorable reconsideration is believed to be in order.

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In view of the above, each of the claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Applicant believes no fee is due with this request. However, if a fee is due, please charge our Deposit Account No. 09-0458, under Order No. 20136-00305-US from which the undersigned is authorized to draw.

Dated: April 26, 2004

Respectfully submitted,

By 

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